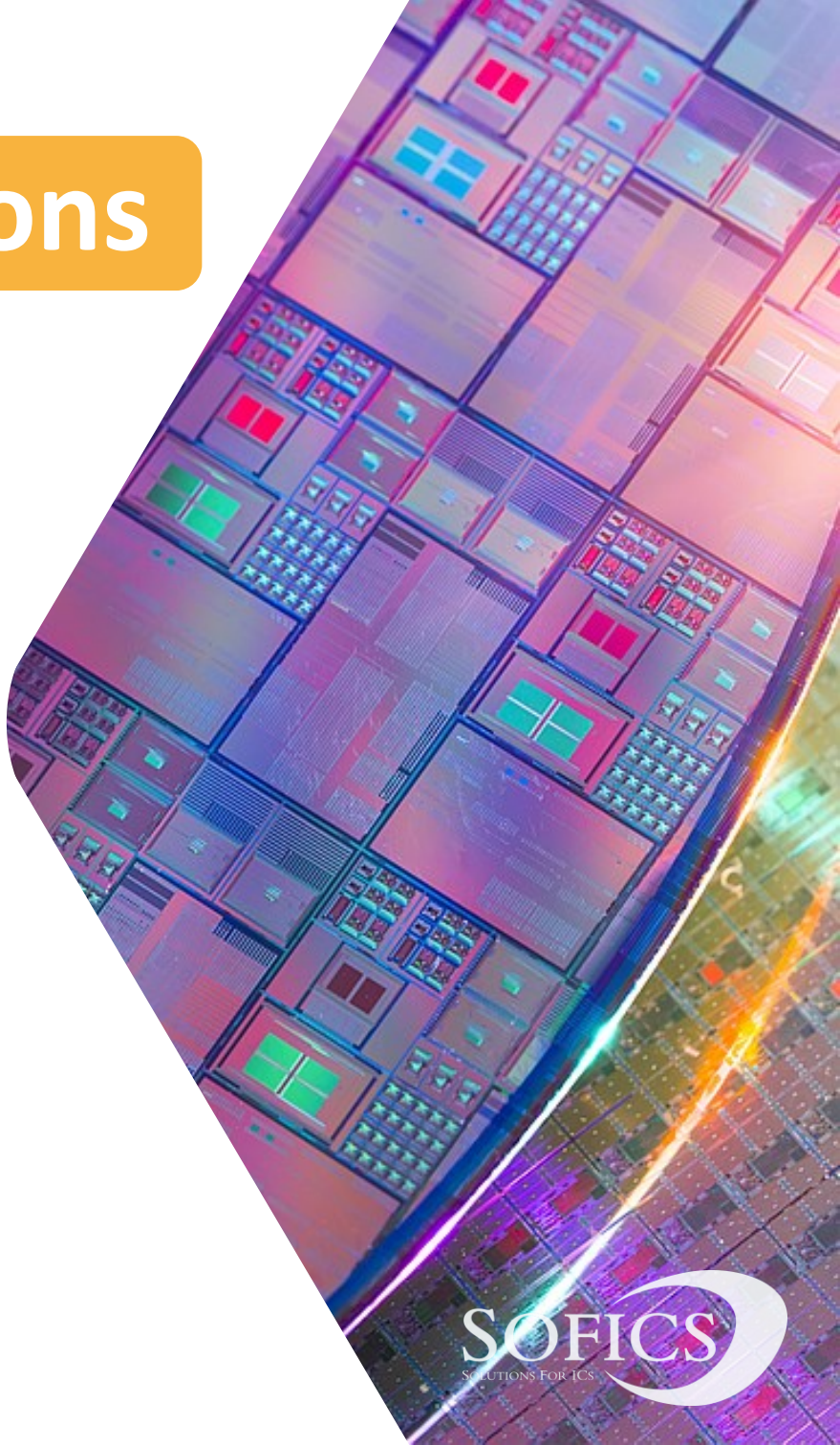
5 key reasons

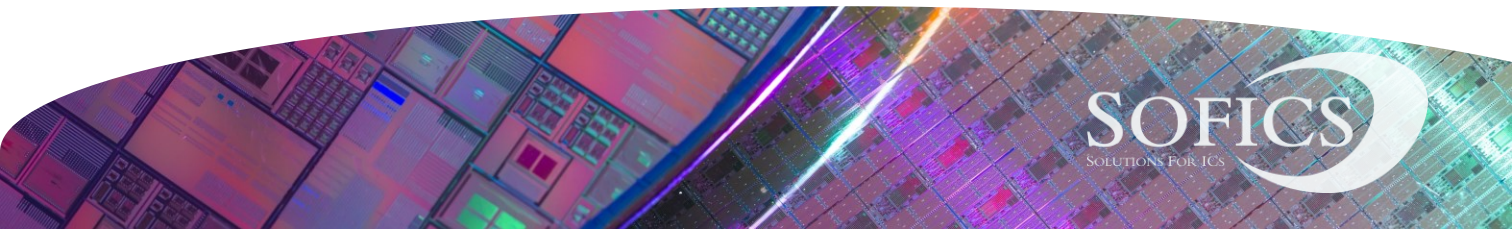
die-2-die interfaces need specialty I/O and ESD



1

‘die-2-die’ (D2D) interfaces operate outside the typical GPIO range

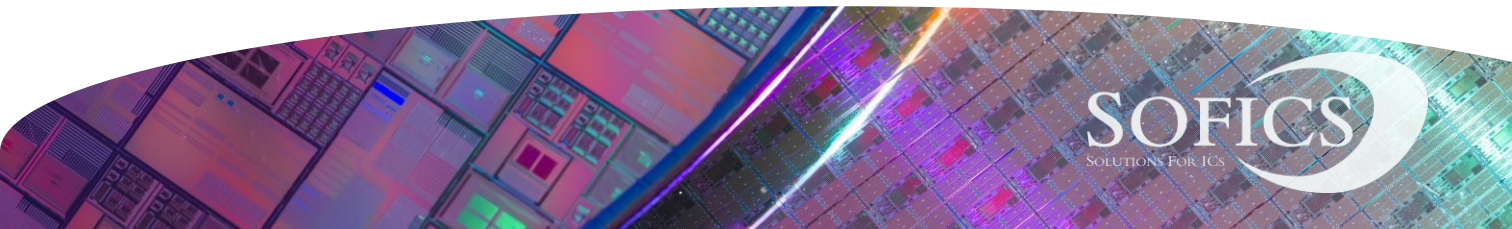
lower signal voltage & reduced drive current



2

For speed, D2D interfaces are designed with thin oxide transistors

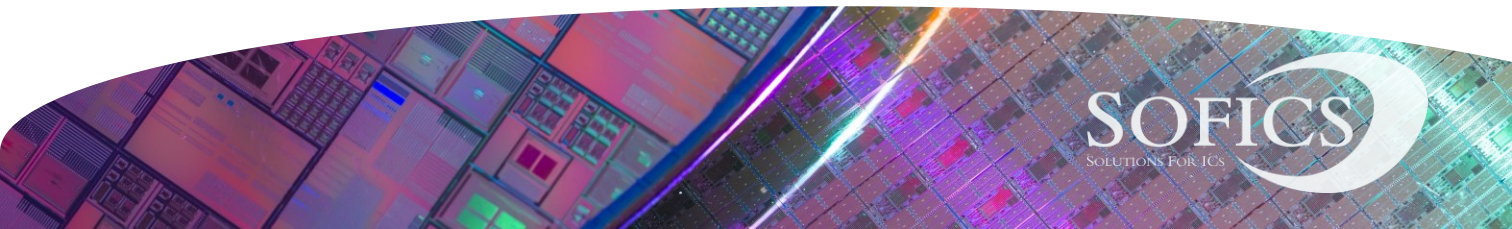
but those are easily damaged during ESD events



3

The parasitic capacitance of ESD protection in traditional GPIOs is too high

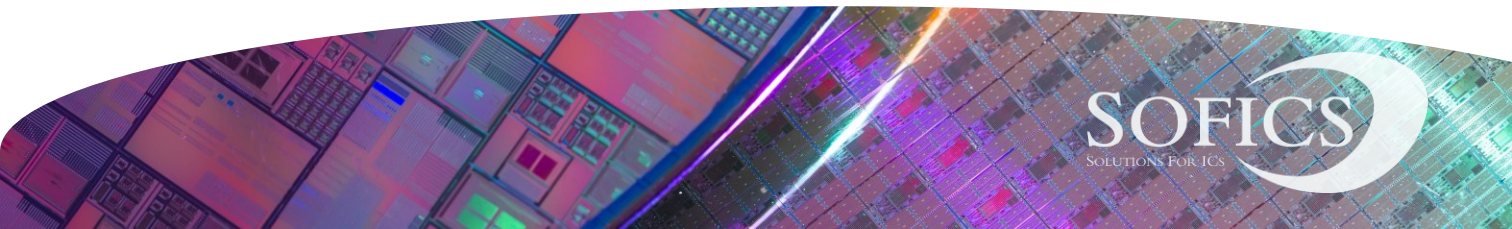
for high bandwidth D2D interfaces



4

When chiplet applications target thousands of D2D connections

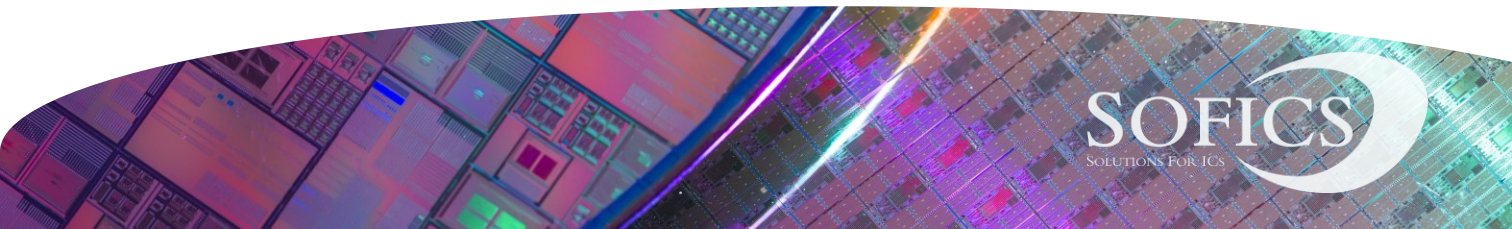
the standard I/O pads consume too much silicon area



5

ESD clamps integrated in traditional GPIOs are designed for >2kV HBM

while D2D interfaces only need a fraction of that.

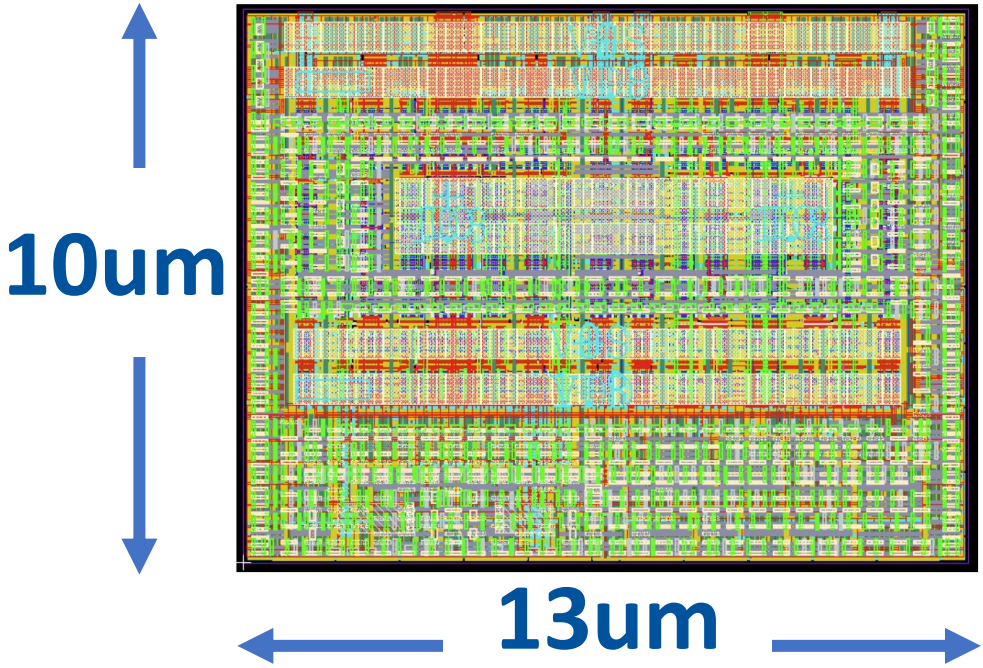


Sofics proven approach

- ESD protection of sensitive thin oxide circuits
- Protection for interfaces at 1V or lower
- ESD protection in smaller area
- Much reduced parasitic capacitance
- Scalable ESD robustness
- Proven on many fabs, processes

Example on 5nm FinFET

Full local protection for 0.9V I/O
>100V HBM
14fF total capacitance



SOFICS
SOLUTIONS FOR ICs

Reach out

- For more examples on other processes
- To discuss your project

Ehsan

Bart

SOFICS
SOLUTIONS FOR ICS